4. (a) Design a BCD-to-Excess 3 code converter using minimum number of NAND gates.

   (b) Write down the procedure to convert a given AND-OR gate network to all NAND gates network. 8+2

5. (a) Implement the logic expression $f = \sum m\ (0, 2, 5, 7)$ by 1:8 demultiplexer.

   (b) Design a two-bit comparator by discrete logic gates. 4+6

6. (a) Design S-R flip-flop using NAND gates only.

   (b) Convert it to J-K flip-flop.

   (c) Can a D flip-flop be made to operate in the toggle mode? 4+4+2

7. (a) Design a counter with counting sequence 0–3–5–1–7–6–0... using J-K flip-flops and other logic gates.

   (b) Can a counter be made to start count from any pre-defined value?— Explain. 8+2

8. (a) Design an asynchronous MOD-4 DOWN counter.

   (b) Find the outputs of the key diode matrix circuit in Figure (1), where the input keys are pressed one at a time, K_0, K_1, K_2 are press to **ON** switch, D_0 to D_6 are PN Junction diode, R_0 to R_3 are resistors and Y_0 to Y_3 are outputs. Justify your answer.

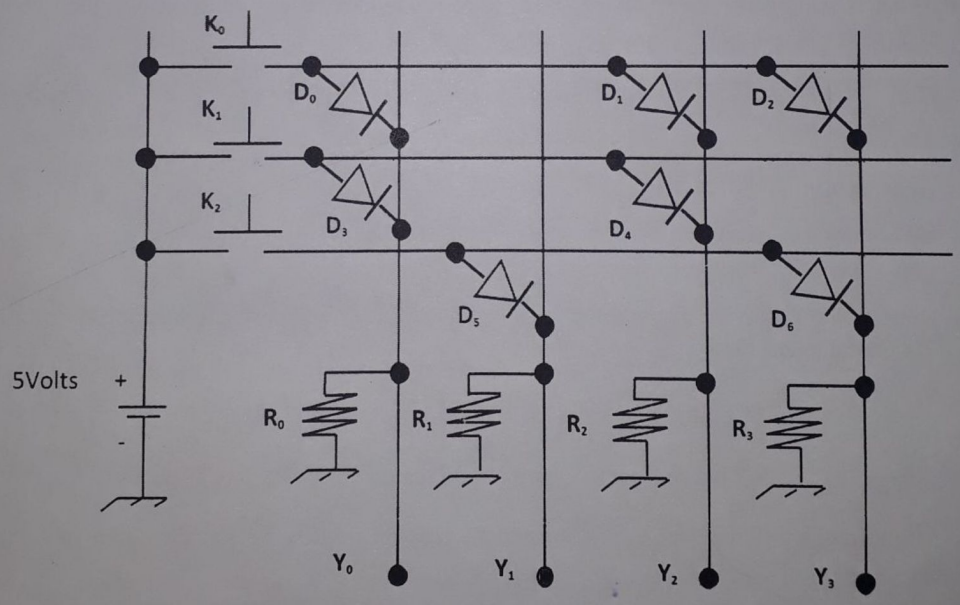

Figure (1)

   (c) What is the 'race-around' condition in a J–K flip-flop? 5+3+2

2018

COMPUTER SCIENCE – HONOURS

Paper : CC-1

Full Marks : 50

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

Answer ***Question no.*** **1** and ***any four*** from the rest.

1. Answer ***any five*** questions from the following : 2×5

(a) Find the maxterm of $f(x, y, z) = xy + yz + zx$.

(b) Draw the truth table for : $(A'+B) \oplus (A+B')$.

(c) Compare between positive and negative edge-triggerred clock pulses.

(d) Convert the number $(DEC.A)_{16}$ to decimal.

(e) How many bits are required to represent decimal values ranging from –50 to +50?

(f) What is weighted code? Differentiate between weighted codes and non-weighted codes.

(g) Add : (i) $(35)_8 + (53)_8$; (ii) $(9F)_{16} + (BA)_{16}$.

(h) Subtract $(0111)_2$ from $(0011)_2$ using 1's complement method and also using 2's complement method.

2. (a) Convert :

(i) $(11001111 \cdot 1010)_2 = (?)_8$

(ii) $(3A \cdot 2F)_{16} = (?)_2$

(iii) $(396 \cdot 82)_{10} = (?)_2$

(b) Convert the following decimal numbers to signed binary and perform the addition/subtraction using 2's complement method.

(i) 33 + 15

(ii) 56 – 27

(c) Design Y_{diff} of a 3-bit full subtractor by NOR gates only. 3+3+4

3. (a) Minimize the following logic function and realize using logic gates having minimum number of levels.

$f = \sum m\,(1, 3, 5, 8, 9, 11, 15) + \sum d\,(2, 13)$

Draw the truth table.

(b) Make a 4-input NAND gate using 2-input NAND gates.

(c) Realize Exclusive-OR logic function using minimum number of two-input NAND gates only.

5+3+2

Please Turn Over