2021

ELECTRONICS — HONOURS

Paper : DSE-A-1

(Basic VLSI Design)

Full Marks : 50

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

Answer ***question no.*** **1** and ***any four*** from the rest of the questions.

1. Answer ***any ten*** questions of the following : 1×10

(a) MOS Transistors consist of which of the following?

(i) Semiconductor Layer (ii) Metal Layer

(iii) Layer of SiO_2 (iv) All of these.

(b) In n-channel MOSFET, which is the more negative element?

(i) Source (ii) Gate

(iii) Drain (iv) Substrate.

(c) CMOS has _____ .

(i) high noise margin (ii) high packing density

(iii) high power dissipation (iv) high complexity

(d) What is the disadvantage of MOS device?

(i) Limited current sourcing (ii) Limited voltage sinking

(iii) Limited voltage sourcing (iv) Unlimited current sinking.

(e) What are the advantages of BiCMOS?

(i) Higher gain (ii) High frequency characteristics

(iii) Better noise characteristics (iv) All of the mentioned.

(f) BiCMOS has low power dissipation.

(i) True (ii) False

(g) Which model is used for scaling?

(i) Constant electric scaling

(ii) Constant voltage scaling

(iii) Constant voltage and electric scaling

(iv) Constant current model.

(h) In basic inverter circuit, _____ is connected to gound.

(i) Source (ii) Drain

(iii) Gate (iv) Body.

(i) Which of the following is not a type of memory?

(i) RAM (ii) FPROM

(iii) EEPROM (iv) ROM.

(j) The Chip by which both read and write operation can be performed is

(i) RAM (ii) ROM

(iii) PROM (iv) EPROM.

(k) The VIL is found from the transfer characteristics of inverter by

(i) the point where straight line at VOH ends.

(ii) the slope of the transition at a point at which the slope is -1.

(iii) the midpoint of the transition line.

(iv) All of these.

(l) A latch is an example of

(i) Monostable multivibrator (ii) Astable multivibrator

(iii) Bistable multivibrator (iv) 555 Timer.

2. Draw the schematic of a SRAM cell and explain its operation. Compare SRAM, DRAM and Flash memory in terms of cell size, writing speed, compatibility with basic CMOS technology and application. 2+4+4

3. Draw the equivalent circuit of level 1 MOSFET model in SPICE and explain different components. Explain, how the effective channel length, gate-source overlap distance can be obtained in SPICE. Draw and explain the output characteristics with the variation of T_{OX} for level 1 model. 4+2+4

4. Draw the general circuit diagram of a nMOS inverter and explain the typical voltage transfer characteristics from it. Define V_{OH}, V_{OL}, V_{IL} and V_{IH} with respect to an inverter circuit. 2+4+4

5. Write short notes on : 5+5

(a) Enhancement load nMOS inverter

(b) Depletion load nMOS inverter.

6. Discuss in brief on RC delay model and the Elmore delay model in connection with interconnect delay and highlight the difference between the two. 4+4+2

7. Draw the circuit structure of a simple CMOS S-R Latch and explain its operation in details. Draw the circuit diagram of a CMOS J-K latch and explain how toggle state can be avoided for J= K= 1. 3+4+3

8. (a) What are the factors that causes Static and Dynamic power dissipation in CMOS circuits?

(b) What is pass transistor logic? Implement Ex-OR gate using pass transistor.

(c) What is meant by a transmission gate?

(d) Draw the BiCMOS inverter circuit. 3+3+2+2
