T(2nd Sm.)-Electronics-G/GE/CC-2/CBCS

2021

ELECTRONICS — GENERAL

Paper : GE/CC-2

(Linear and Digital Integrated Circuits)

Full Marks : 50

The figures in the margin indicate full marks. Candidates are required to give their answers in their own words

as far as practicable.

Answer question no. 1 and any four questions, taking at least one question from each Unit.

1. Answer any ten questions :

- (a) Characteristics of an ideal OP-AMP is/are (i) infinite input impedance (ii) zero output impedance (iii) infinite voltage gain (iv) All of these. (b) CMRR of an ideal OP-AMP is (i) Infinite (ii) Zero (iii) One (iv) 10. (c) A monostable multivibrator using IC 555 timer requires (i) an optimum input signal at threshold pin (ii) an optimum input signal at trigger pin (iii) no signal at trigger pin (iv) None of these. (d) Calculate the output voltage of an OP-AMP as summing amplifier for three inputs : V1 = 1V, V2 = -2V, V3 = 3V. Assume, all resistance connected in the circuit as 1 K Ω . (i) -2V (ii) 2V (iii) 2000V (iv) -2000V. (e) The decimal equivalent of the binary number 1010.011 is (ii) 10.10 (i) 10.5 (iii) 10.375 (iv) 10.75.
- (f) The Boolean expression x(x + y) is equal to
 - (ii) x + x.y(i) x
 - (iii) x.y (iv) y.

Please Turn Over

1×10

T(2nd Sm.)-Electronics-G/GE/CC-2/CBCS (2) (g) Weighted code among the following is/are (i) 8421 (ii) Excess-3 (iii) Gray code (iv) ASCII. (h) A MOD-8 counter can be designed using (i) 5 flip flop (ii) 2 flip flop (iii) 4 flip flop (iv) 3 flip flop. (i) Which of the following logic gate(s) provide zero output for equal inputs? (i) OR (ii) NOR (iv) Ex-OR. (iii) NAND (j) A full Adder can be designed using (i) two-half adder and a NOR gate (ii) two-half adder and an OR gate (iii) two-half adder and a NAND gate (iv) two-half adder and an AND gate. (k) J and K inputs are _____, when toggle state arises. (i) Both high (ii) Both low (iii) J-high; K-low (iv) K-high; J-low. (l) Resolution is (i) inversely proportional to total number of steps. (ii) directly proportional to total number of steps. (iii) independent of total number of steps. (iv) None of the above.

Unit - I

- 2. (a) Draw the schematic diagram of an integrator circuit using OP-AMP and analyse its performance.
 - (b) Explain OP-AMP as a differential amplifier.
 - (c) What is slew rate?
- 3. (a) Explain the term virtual ground in connection with an OP-AMP.
 - (b) What do you mean by frequency response of an OP-AMP?
 - (c) How can an OP-AMP be used as a non-inverting amplifier? Find the expression for its voltage gain. 2+3+5

4+4+2

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(3) Unit - II

4.	(a)	Perform $(1011 - 1101)_2$ by 2's complement method.	
	(b)	Find the complement of the following function :	
		$\mathbf{F} = (\mathbf{x}'\mathbf{y}\mathbf{z}' + \mathbf{x}'\mathbf{y}'\mathbf{z})$	
	(c)	Simplify the following expression using Karnaugh Map :	
		$F(A,B,C,D) = \sum m(0,1,2,4,5,6,8,9,12,13,14).$	2+3+5
5.	(a)	Design a 4:16 decoder using two 3:8 decoders and give the truth table.	
	(b)	Why is a multiplexer called data selector?	
	(c)	How can you use Ex-OR gate as a controlled inverter?	5+2+3
6.	(a)	Draw a logic block diagram of 4:1 multiplexer and explain its operation.	
	(b)	Implement a full adder circuit by using NAND gates. Give the truth table.	5+5
Unit - III			
7.	(a)	State the difference between combinational and sequential logic systems.	
	(b)	Draw the circuit of a MOD-6 counter and explain its operation.	
	(c)	What is race around condition? How can it be eliminated?	2+5+3
8.	(a)	Draw a D-type flip flop using NAND gates and write down its truth table.	
	(b)	Draw and explain the circuit of a 4-bit shift register with serial loading.	5+5