## 2021

## ELECTRONICS - HONOURS

Paper : CC-9

## (Digital Electronics and VHDL)

## Full Marks : 50

The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words
as far as practicable.
Answer question no. 1 and any four questions from the rest, taking at least one from each unit.

1. Answer any ten questions of the following:
(a) The octal equivalent of $(10110.01)_{2}$ is
(i) $(24.2)_{8}$
(ii) $(25.1)_{8}$
(iii) $(26.2)_{8}$
(iv) $(27.1)_{8}$.
(b) The 2 's complement of the binary number 1010 is
(i) 1101
(ii) 0110
(iii) 0101
(iv) 0111.
(c) Which of the following can represent $(-27)_{10}$ as 7 -bit signed magnitude binary number?
(i) $(1011011)_{2}$
(ii) $(0011011)_{2}$
(iii) $(1101011)_{2}$
(iv) $(0101011)_{2}$.
(d) In BCD system, each decimal digit is represented by a binary number consisting of
(i) 1-bit
(ii) 2-bits
(iii) 3-bits
(iv) 4-bits.
(e) Which of the following is not valid rule of Boolean algebra?
(i) $\mathrm{A}+1=1$
(ii) $\mathrm{A}+0=0$
(iii) $\mathrm{A} .1=1$
(iv) $\mathrm{A} . \mathrm{A}=\mathrm{A}$.
(f) The logical expression $\mathrm{Y}=\mathrm{A}+\overline{\mathrm{A}} \mathrm{B}$ is equivalent to
(i) $\mathrm{Y}=\mathrm{AB}$
(ii) $\mathrm{Y}=\overline{\mathrm{A}} \mathrm{B}$
(iii) $\mathrm{Y}=\mathrm{A}+\mathrm{B}$
(iv) $\mathrm{Y}=\overline{\mathrm{A}}+\mathrm{B}$.
(g) Which of the following uses the least power?
(i) CMOS
(ii) TTL
(iii) ECL
(iv) DTL.
(h) The figure of merit of a logic family is given by
(i) product of noise margin and power dissipation
(ii) product of fan out and propagation delay time
(iii) gain-bandwidth product
(iv) product of propagation delay time and power dissipation.
(i) Flip-flops are examples of
(i) Combinational circuits
(ii) Sequential circuit
(iii) Universal gates
(iv) None of these.
(j) Which of the following is an example of volatile memory?
(i) ROM
(ii) PROM
(iii) RAM
(iv) Hard Disk.
(k) In VHDL, Bus is a type of
(i) Signal
(ii) Constant
(iii) Variable
(iv) Driver.
(l) In VHDL, complete description of the circuit to be designed is given in
(i) Entity
(ii) Library
(iii) Architecture
(iv) Configurations.
(m) The most basic form of Behavioural modelling in VHDL is
(i) IF statements
(ii) Assignment statements
(iii) Loop statements
(iv) WAIT statements.

## Unit - 1

2. (a) Convert the following :
(i) $(57.625)_{10}=(?)_{2}$
(ii) $(10111.0110)_{2}=(?)_{10}$
(iii) $(\mathrm{C} 5 \mathrm{~B})_{16}=(?)_{8}$.
(b) Subtract $(10101)_{2}$ from $(11011)_{2}$ using 2's complement method.
(c) Convert the binary code (10110) into its equivalent Gray code.
3. (a) Why NAND gate is called a universal gate?
(b) Write the truth table of EX-OR gate. Draw the circuit of an EX-OR gate using NAND gates only.
(c) Simplify the following expression using Boolean algebra :

$$
Y(A, B, C)=\bar{A} \bar{B} \bar{C}+A \bar{B} \bar{C}+\bar{A} B \bar{C}+A B \bar{C}
$$

(d) Compare the ECL, TTL \& CMOS logic families based on their fan out, power dissipation and propagation delay.

## Unit - 2

4. (a) What is the main function of Multiplexer?
(b) Construct NOT, NAND and EX-OR gate using 2:1 MUX.
(c) Implement the function $F(A, B, C, D)=\Sigma m(0,2,3,4,8,10,14)$ using 8:1 MUX or 4:1 MUX.

$$
1+(2+2+2)+3
$$

5. (a) What are the differences between latch and flip-flops?
(b) Draw the circuit and write the truth table of an S-R flip-flops and NAND gates. How can you convert it to a D-type flip-flops?
(c) What is race around condition? How can be it eliminated?
6. (a) What do you mean by an asynchronous ripple counter?
(b) Design a 4 bit asynchronous counter using J-K flip-flops. Explain its operating principle.
(c) What do you mean by edge-triggered clock pulse?

## Unit - 3

7. (a) What is Library?
(b) What are the purpose of - (i) the Entity Declaration and (ii) the Architecture body in VHDL.
(c) How many ways can one write VHDL code in the Architecture Body?
(d) List different sequential statements used in VHDL.
8. (a) Discuss the different Data types and Operators in VHDL.
(b) Draw the schematic diagram of a 2:4 decoder. Write its Entity and describe its Behavioural model in VHDL.
(c) What is the concurrent signal assignment?
