

2021

## COMPUTER SCIENCE — HONOURS

Paper : CC-1

(Digital Logic)

Full Marks : 50

*The figures in the margin indicate full marks.**Candidates are required to give their answers in their own words as far as practicable.*Answer **question no. 1** and **any four** questions from the rest.

1. Answer **any five** questions of the following : 2×5
- State De Morgan's theorems.
  - Convert  $(3EA.1D)_{16} = (?)_2 = (?)_8$ .
  - Add  $(11101.101)_2 + (1001.11)_2$  and  $(6D.C)_{16} + (3B.2)_{16}$ .
  - Design EX-OR gate by NAND gates only.
  - Subtract  $(1011)_2 - (1101)_2$  using 2's complement.
  - Which type of topology has been adopted to overcome race around condition? Explain.
  - What are the differences between multiplexer and demultiplexer?
  - How many flip-flops and other logic gates are required to design an UP decade counter?
2. (a) Simplify the logic expression  $F = \sum m(0, 2, 5, 7, 8, 10, 13, 15)$  by K-map method. Design the circuit following simplified expression. Draw the truth table.
- (b) Identify the maxterms from the above mentioned logic expression. Simplify it by K-map method. 7+3
3. (a) Implement  $Y_{\text{difference}}$  output of a 3-bit full subtractor by the logic gates. Draw the truth table.
- (b) Implement  $Y_{\text{carry}}$  output of a 3-bit full adder by NAND gates only. 6+4
4. (a) Implement  $Y = \sum m(0, 4, 5, 6, 9, 10, 13, 14)$  by 8:1 multiplexer. Draw the truth table.
- (b) Implement  $Y_{\text{sum}}$  output of a half adder by demultiplexer. 7+3
5. (a) Design a 2-bit multiplier by multiplying  $(10)_2$  and  $(11)_2$ .
- (b) Draw the necessary truth table. 8+2

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6. (a) What is Set-Reset flip-flop? Design it by NAND gates only and explain. Draw the truth table. 5+2+3
- (b) What is race around condition?
- (c) How can the Set-Reset flip-flop be converted into D-flip-flop? Draw the truth table of D-flip-flop. 5+2+3
7. (a) Design an asynchronous UP decade counter. Explain its function. 6+4
- (b) Design a MOD-5 counter showing all the count sequence. 6+4
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