2022

ELECTRONICS — HONOURS — PRACTICAL

Paper : CC-8P

(Operational Amplifiers and Applications)

Full Marks : 30

The figures in the margin indicate full marks.

Marks Distribution

- Laboratory Notebook : 05
- Viva : 07
- Experiment : 18

Answer ***any one*** question.

1. (a) Design an amplifier with voltage gain 10 for an inverting configuration using an op-amp. Take at least 8 readings and draw the graph.
[Theory - 2, Design - 2, Circuit drawing - 1, Apparatus - 1, Data collection - 2, Graph - 2] 10

(b) Design a voltage follower using an op-amp. Take at least 8 readings and draw the graph.
[Theory - 2, Circuit drawing - 1, Apparatus - 1, Data collection - 2, Graph - 2] 8

2. (a) Design an amplifier with voltage gain 5 for a non-inverting configuration using an op-amp. Take at least 8 readings and draw the graph.
[Theory - 2, Design - 2, Circuit drawing - 1, Apparatus - 1, Data collection - 2, Graph - 2] 10

(b) Design a unity gain buffer using an op-amp. Take at least 8 reading and draw the graph.
[Theory - 2, Circuit drawing - 1, Apparatus - 1, Data collection - 2, Graph - 2] 8

3. (a) Design an analog adder with 3 voltage inputs using an op-amp. Take at least 8 readings. Compare the experimental result with the theoretical result and comment on it.
[Theory - 2, Design - 2, Circuit drawing - 1, Apparatus - 1, Data collection - 2, Graph - 2] 10

(b) Design a unity gain buffer using an op-amp. Take at least 8 reading and draw the graph.
[Theory - 2, Circuit drawing - 1, Apparatus - 1, Data collection - 2, Graph - 2] 8

4. (a) Design an analog subtractor using an op-amp. Take at least 8 readings. Compare the experimental result with theoretical and comment on it.
[Theory - 2, Design - 2, Circuit drawing - 1, Apparatus - 1, Data collection - 2, Graph - 2] 10

(b) Design a voltage follower using an op-amp. Take at least 8 reading and draw the graph.
[Theory - 2, Circuit drawing - 1, Apparatus - 1, Data collection - 2, Graph - 2] 8

5. Design a first-order low-pass filter using op-amp having a cut-off frequency of 5 kHz and passband voltage gain 2. Collect necessary data to plot frequency vs gain curve. Compare the experimental result (cut-off frequency and passband gain) with theoretical values and comment on it.
[Theory - 2, Design - 2, Circuit drawing - 2, Apparatus - 1, Data collection - 5, Graph - 4, Comparison - 2] 18

6. Design a first-order high-pass filter using op-amp having a cut-off frequency of 1 kHz and passband voltage gain 4. Collect necessary data to plot frequency vs gain curve. Compare the experimental result (cut-off frequency and passband gain) with theoretical values and comment on it.
[Theory - 2, Design - 2, Circuit drawing - 2, Apparatus - 1, Data collection - 5, Graph - 4, Comparison - 2] 18

7. Design an RC Phase shift oscillator using op-amp for a given frequency of 1 kHz and observe the output waveform in a CRO. Draw a graph of the output waveform from the relevant data obtained from the CRD. Measure the frequency of the waveform.
[Theory - 2, Design - 2, Circuit drawing - 2, Apparatus - 2, Data collection - 4, Graph - 4, Measurement - 2] 18

8. Design an Wien Bridge oscillator using op-amp for a given frequency of 2 kHz and observe the output waveform in a CRO. Draw a graph of the output waveform from the relevant data obtained from the CRD. Measure the frequency of the waveform.
[Theory - 2, Design - 2, Circuit drawing - 2, Apparatus - 2, Data collection - 4, Graph - 4, Measurement - 2] 18

9. Design an astable multivibrator using IC 555 for a given frequency of 1 kHz and 50% duty cycle. Observe the output waveform in CRO and draw the graph. Compare the experimental result with theoretical value (frequency and duty cycle) and comment on it.

[Theory - 2, Design - 2, Circuit drawing - 2, Apparatus - 2, Data collection - 4, Graph - 4, Measurement - 2] 18

10. Construct and study the adjustable voltage regulator (10V) using fixed voltage regulator IC7805. Vary input voltage from 12V to 30V and record the output voltages. Vary the load resistance in steps (by keeping input voltage constant) and measure the regulator output and plot the graph.

[Theory - 2, Design - 2, Circuit drawing - 2, Apparatus - 3, Data collection - 5, Graph - 4] 18

2022

ELECTRONICS — HONOURS — PRACTICAL

Paper : CC-9P

(Digital Electronics and VHDL)

Full Marks : 30

The figures in the margin indicate full marks.

Marks Distribution :

- Laboratory Notebook : 05
- Viva voce : 07
- Experiment : 18

Candidate has to perform ***one*** of the following experiments.

1. Design OR, AND and NOT gates using NAND gates only and verify their truth table.

[Theory — 2+2+1, Circuit design and implementation — 2+2+1, Record of Data — 2+2+1, Discussion — 1+1+1] 18

2. *(a)* Design the following Boolean identity using basic gates

$$(A + B).(A+C) = A + BC$$

Also verify their truth table. The outputs are to be measured in volts.

[Theory — 2, Circuit design and implementation — 4, Record of Data — 3, Discussion — 1]

(b) Design XOR gate using NAND gates only and verify its truth table.

[Theory — 2, Circuit design and implementation — 3, Record of Data — 2, Discussion — 1]. 18

3. (a) Design the following Boolean identity using basic gates

$$AB + \bar{A}C = (A + C).(\bar{A} + B)$$

Also verify the truth tables. The outputs are to be measured in volts.

[Theory — 2, Circuit design and implementation — 4, Record of Data — 3, Discussion — 1]

(b) Design XOR gate using basic gates and verify its truth table.

[Theory — 2, Circuit design and implementation — 3, Record of Data — 2, Discussion — 1]

18

4. (a) Construct a half-adder circuit using minimum number of NAND gates and verify its truth table. The outputs are to be measured in volts.

[Theory — 2, Circuit design and implementation — 3, Record of Data — 2, Discussion — 1]

(b) Construct a full-adder circuit using basic gates and verify its truth table. The outputs are to be measured in volts.

[Theory — 2, Circuit design and implementation — 4, Record of Data — 3, Discussion — 1]

18

5. (a) Construct a half-subtractor circuit using NAND gates and verify its truth table. The outputs are to be measured in volts.

[Theory — 2, Circuit design and implementation — 3, Record of Data — 2, Discussion — 1]

(b) Construct a full-subtractor circuit using basic gates and verify its truth table. The outputs are to be measured in volts.

[Theory — 2, Circuit design and implementation — 4, Record of Data — 3, Discussion — 1]

18

6. (a) Design a 4 : 1 multiplexer circuit using NAND gates and verify its truth table. The outputs are to be measured in volts.

[Theory — 3, Circuit design and implementation — 4, Record of Data — 3, Discussion — 1]

(b) Verify the following Boolean identity using basic gates

$$A + \bar{A}B = A + B$$

[Theory — 2, Circuit design and implementation — 2, Record of Data — 2, Discussion — 1]

18

7. Construct (i) SR flip-flop and (ii) D-flip-flop using NAND gates and verify their truth tables. The outputs are to be measured in volts.

[Theory — 2+2, Circuit design and implementation — 4+4, Record of Data — 2+2, Discussion — 1+1] 18

8. Use negative edge triggered JK flip-flops to construct a 4-bit ripple counter which counts in the up direction and verify its truth table. The outputs are to be measured in volts.

[Theory — 4, Circuit design and implementation — 7, Record of Data — 5, Discussion — 2] 18

9. Construct a 'Mod-10' asynchronous counter using negative edge-triggered J-K flip-flops and verify its truth table. Outputs are to be measured in volts.

[Theory — 4, Circuit design and implementation — 7, Record of Data — 5, Discussion — 2] 18

10. Write VHDL code to realize OR, AND and NOT gates and verify their truth tables.

[Theory — 2+2+2, VHDL code — 2+2+2, Simulation — 2+2+2] 18

11. Write VHDL code to design half-adder and full-adder circuits and verify their truth tables.

[Theory — 2+3, VHDL code — 3+4, Simulation — 3+3] 18

12. Write VHDL code to design Half-subtractor and Full-subtractor circuits and verify their truth table.

[Theory — 2+3, VHDL code — 3+4, Simulation — 3+3] 18

13. Write VHDL code to design a 4:1 Multiplexer and 2 : 4 Decoder using basic gates and also verify their truth tables.

[Theory — 2+2, VHDL code — 4+4, Simulation — 3+3] 18

2022

ELECTRONICS — HONOURS — PRACTICAL

Paper : CC-10P

(Signals and Systems)

Full Marks : 30

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

Laboratory Notebook	– 5
Viva voce	– 7
Experiment	– 18
Program – 12	
Output – 6	

Answer ***any one*** question.

1. Write a Scilab/Matlab Program to generate the following continuous time signals :

(a) Unit step signal

(b) Sinusoidal signal

(c) Ramp signal.

Program – (4+4+4) = 12; Output – (2+2+2) = 6

2. Write a program in Scilab/Matlab to generate the following discrete time signals :

(a) Unit impulse signal

(b) Unit step signal

(c) Ramp signal.

Program – (4+4+4) = 12; Output – (2+2+2) = 6

3. Write a program in Scilab/Matlab to generate the following signals :

   (a) $x(n+2)$ and $x(n-3)$ when $x(n) = \left\{1, 2, \underset{\uparrow}{3}, 4, 5\right\}$.

   (b) $2x(n)$ when $x(n)$ $\left\{1, 2, \underset{\uparrow}{3}, 4, 5\right\}$.

   Program – (6+6) = 12; Output – (3+3) = 6

4. Write a program in Scilab/Matlab to perform linear convolution of any two given signals [Signals to be provided by the examiner].

   Program – 12; Output – 6

5. Write a program in Scilab/Matlab to perform Fourier transform of any given continuous signal [Signal to be provided by the examiner].

   Program – 12; Output – 6

6. Write a program in Scilab/Matlab to perform Laplace transform of any given continuous time signal.

   Program – 12; Output – 6
