

2022

**ELECTRONICS — HONOURS**

**Paper : CC-9**

**(Digital Electronics and VHDL)**

**Full Marks : 50**

*The figures in the margin indicate full marks.*

*Candidates are required to give their answers in their own words as far as practicable.*

Answer **question no. 1** and **any four** questions from the rest, taking **at least one** from **each Unit**.

1. Answer **any ten** questions :

1×10

(a) What is the BCD equivalent of  $(75)_{10}$ ?

~~(i)~~  $(01110101)_2$

(ii)  $(111101)_2$

(iii)  $(111011)_2$

(iv)  $(01110110)_2$

Handwritten:  $101001011$

(b) Which of the Boolean functions has canonical form?

(i)  $F = \bar{A}\bar{C} + \bar{C}D$

(ii)  $F = \bar{A}B\bar{C} + AB\bar{C}$

(iii)  $F = \bar{B} + AB$

(iv)  $F = ACD + ABC\bar{D}$

Handwritten:  $0110101$

(c) The logical expression  $F = \bar{A}B + A\bar{B}$  is associated to the term.

(i) Inequality checker

(ii) Equality checker

(iii) Odd parity checker

(iv) Even parity checker.

Handwritten:  $00101010$

(d) Multiplexers are

(i) Synchronous sequential circuits

(ii) Asynchronous sequential circuits

~~(iii)~~ Combinational circuits

(iv) None of these.

(e) The correct form of De Morgan's theorem is

(i)  $A \cdot \bar{B} = A + \bar{B}$

(ii)  $\bar{A} + \bar{B} = \bar{A} \bar{B}$

(iii)  $\overline{AB} = \bar{A} + \bar{B}$

~~(iv)~~  $\overline{A + B} = \bar{A} \cdot \bar{B}$

(f) The time between 2 pulses may vary from

(i) 1  $\mu$ sec to 18  $\mu$ sec

(ii) 1  $\mu$ sec to 10  $\mu$ sec

(iii) 1 msec to 10 msec

~~(iv)~~ Can't be said.

Please Turn Over

- (g) Apart from the use in integrated circuits CMOS technology also used in
- (i) Calculators
  - (ii) Wrist watches
  - (iii) Battery driven computers
  - (iv) All of the above.
- (h) Which of the following is the correct order for IC families according to technology?
- (i) RTL, DTL, I<sup>2</sup>L, TTL
  - (ii) TTL, DTL, ECL, I<sup>2</sup>L
  - (iii) RTL, DTL, TTL, ECL
  - (iv) TTL, HTL, RTL, DTL.
- (i) What is a D-FF?
- (i) It is basically a S-R FF with an inverter in the R input.
  - (ii) It is basically a S-R FF with an inverter in the S input.
  - (iii) It is a S-R FF with shorted RS inputs.
  - (iv) It is not at all related to S-R FF.
- (j) A package in VHDL consists of
- (i) Commonly used architectures
  - (ii) Commonly used tools
  - (iii) Commonly used datatypes and subroutines
  - (iv) Commonly used syntax and variable.
- (k) Pre-defined data for an VHDL object is called
- (i) Generic
  - (ii) Constant
  - (iii) Attribute
  - (iv) Library.
- (l) What is the use of the configuration statement?
- (i) To configure the components exactly in design.
  - (ii) To complete the design process by adding libraries.
  - (iii) To add more than one entities into a single architecture.
  - (iv) To add some component in any entity architecture pair.

**Unit - 1**

2. (a) Convert decimal number 52.89 to hexadecimal.
- (b) Subtract the BCD numbers (73-56).
- (c) Prove De Morgan's theorems using Boolean algebra.
- (d) Write down the truth table of NAND gate.

$$2+3+(2+2)+1$$

3. (a) Simplify following Boolean function using K-Map.  $F = \sum m (1, 5, 7, 11, 15)$  with a don't care function  $D = \sum m (3, 9, 12)$ .

- (b) What is meant by noise immunity?
- (c) Briefly explain totem pole connection in TTL.

$$\overline{A \cdot B} = \overline{A} + \overline{B}$$

$$\overline{A} (B + \overline{B}) +$$

5  
6

(3)

Unit - II

- 4. (a) What is a decoder? Why is it also called as minterm generator?
- (b) What is the significance of the term 'half' in 'half-adder'? How can a full-adder be constructed by cascading two half-adders?
- (c) What is an encoder? (1+2)+(2+3)+2
- 5. (a) Compare between combinational logic circuit and sequential logic circuits.
- (b) Explain the operation of J-K FF with diagram. Also write down its truth table.
- (c) Convert J-K FF to T-FF.
- (d) Write down any two basic features of clock pulses. 3+(2+1+1)+2+1
- 6. (a) Compare between synchronous and asynchronous counters.
- (b) Design a 8-bit ring counter and describe its working principle.
- (c) What is a shift register? 2+(3+3)+2

Unit - III

- 7. (a) Define an entity in VHDL.
- (b) What is sequential statements?
- (c) What is the most basic form of behavioral modelling in VHDL?
- (d) What is a sensitivity list?
- (e) Compare between inertial delay and transport delay. 2+2+1+2+3
- 8. (a) Write down some important features of VHDL.
- (b) What is the importance of delay in VHDL?
- (c) Is VHDL a structured software?
- (d) What does => mean in VHDL?
- (e) What is process declarative region and process statement region? 2+2+1+1+(2+2)

