2022

ELECTRONICS — HONOURS

Paper : DSE-A-1

(Basic VLSI Design)

Full Marks : 50

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

Answer ***question no.* 1** and ***any four*** questions from the rest.

1. Answer ***any ten*** questions : 1×10

(a) Speed power product is measured as the product of

(i) gate switching delay and gate power dissipation

(ii) gate switching delay and gate power absorption

(iii) gate switching delay and net gate power

(iv) gate power dissipation and absorption.

(b) nMOS devices are formed in

(i) p-type substrate of high doping level

(ii) n-type substrate of low doping level

(iii) p-type substrate of moderate doping level

(iv) n-type substrate of high doping level.

(c) In a Depletion MOSFET

(i) a channel is always present (ii) a channel is induced

(iii) there is no p-n junction (iv) the gate is not insulated.

(d) The voltage that turns on an E-MOSFET is called

(i) Pinch off voltage (ii) Threshold voltage

(iii) Cutin voltage (iv) Breakdown voltage.

(e) nMOS is

(i) donor doped (ii) acceptor doped

(iii) all the above (iv) none of the above.

(f) VLSI technology uses _____ to form integrated circuit.

(i) transistors (ii) switches

(iii) diodes (iv) buffers.

(g) CMOS devices uses

(i) a JFET and a BJT (ii) D-MOS devices

(iii) Two BJT devices (iv) one nMOS and one pMOS.

(h) Dynamic power dissipation of a CMOS inverter depends on the

(i) power supply voltage (ii) channel width of n-MOS

(iii) channel width of pMOS (iv) All of these.

(i) CMOS inverter has _____ regions of operations.

(i) two (ii) three

(iii) four (iv) five.

(j) RAM is a _____ cell.

(i) static (ii) pseudo static

(iii) dynamic (iv) partially dynamic.

(k) α is used for scaling

(i) linear dimensions (ii) V_{dd}

(iii) oxide thickness (iv) non-linear.

(l) The noise immunity of a inverter circuit _____ with noise margin.

(i) increases (ii) decreases

(iii) constant (iv) None of these.

2. (a) Why NMOS technology is preferred more than PMOS technology?

(b) What is channel length modulation?

(c) Define threshold voltage in CMOS.

(d) What are the advantages of CMOS process? 2+3+2+3

3. (a) What is BiCMOS Technology?

(b) What are the basic processing steps involved in BiCMOS process?

(c) What are the basic differences between level 1 and level 2 SPICE model.

(d) Explain the variation of drain current with parameter 'GAMMA' for level 2 model. 2+3+2+3

4. (a) Explain the operation of a CMOS inverter with a proper circuit diagram.

(b) Draw the inverter characteristic curve and explain the various region in the curve.

(c) What is CMOS noise margin? 4+4+2

5. (a) Explain the different mechanism of power dissipation in a CMOS circuit.
   (b) Draw the lumped RC equivalent circuit of a chain of four pass transistor driving a capacitive load.
   (c) Draw the circuit of a CMOS D-latch (version-1) and explain its operation.
   (d) State the advantages of transmission gates. 2+3+4+1

6. (a) Explain 3-transistor dynamic RAM cell with schematic diagram.
   (b) In what way the DRAMs differ from SRAMs?
   (c) What are Interconnect Delay and Clock Distribution? 4+2+(2+2)

7. (a) Draw and explain the operation of a 2 input NOR gate layout.
   (b) Draw the circuit diagram of a depletion load nMOS SR latch circuit based on 2 input NOR gates and explain its operation. (2+3)+(2+3)

8. Write short notes on ***any two*** of the following : 5+5
   (a) Dynamic logic circuits
   (b) Read Only Memory (ROM) circuit
   (c) Dynamic Read Write Memory (DRAM) circuit
   (d) Monostable sequential circuit.

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