2024

COMPUTER SCIENCE — HONOURS

Paper : DSE-A-3 and DSE-A-4

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

DSE-A-3

(Embedded Systems)

Full Marks : 50

Answer ***question no.*** **1** and ***any four*** from the rest.

1. Answer ***any five*** questions : 2×5

(a) Highlight any four main application areas of Microcontrollers.

(b) What is Harvard Architecture? Is the MCS-51 based on Harvard Architecture? Justify your answer.

(c) What is the procedure of selecting the Register Banks of data memory of MCS-51 (Intel 8051) using PSW?

(d) Briefly explain the purpose of PCON special function register with proper illustrations.

(e) What is the purpose of using Program Lock bits in MCS-51 (Intel 8051)?

(f) What is Register Indirect Addressing? Briefly explain with suitable example with respect to MCS-51 (Intel 8051).

(g) Explain the working of the instruction MOV C, bit associated with MCS-51 (Intel 8051).

(h) How are hardware described in VHDL?

2. (a) Explain the operation of MOVC A, @A + PC instruction of MCS-51 with proper illustrations.

(b) Discuss different methods for moving contents of register R2 to R1 (Assume that register bank 0 of data memory is selected). The direct address of Register R1 and R2 are 01H and 02H respectively. 5+5

3. (a) What is the purpose of Program Store Enable $\overline{(\text{PSEN})}$ and External Access $\overline{(\text{EA})}$?

(b) Explain the purpose of subroutine and execution of LCALL with respect to MCS-51. (2+2)+(2+4)

4. (a) Draw the block diagram of MCS-51 (Intel 8051) and explain the working of each block in brief.

(b) Highlight at least five different main differences between Microcontrollers and Microprocessors. (2+3)+5

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5. (a) Explain the purpose and working of Accumulator, Register-B and Stack Pointer.

   (b) Write short notes on the Bit addressable memory that are available in MCS-51 and why it is important. 6+4

6. (a) Highlight the main differences between PAL and FPGA.

   (b) Implement the following SOP using a PLD with two input lines designated as A, B and outputs O_1, O_2, O_3 and O_4. Draw the appropriate schematic diagram of

   $O_1 = \overline{A}.B + \overline{A}.\overline{B}$

   $O_2 = 0$

   $O_3 = A.B$

   $O_4 = 1$. 6+4

7. (a) Explain the purpose of Interrupt Service Routine (ISR).

   (b) Explain the handling of Interrupts of MCS-51 (Intel 8051) with the help of Special function registers TCON, IE and IP. 4+6

8. (a) What are the Port registers? Why are they important?

   (b) Draw the internal schematic diagram of Port-0 of MCS-51 and explain its working. (1+2)+(3+4)