2023

COMPUTER SCIENCE — HONOURS — PRACTICAL

Paper : CC-1P

Full Marks : 30

The figures in the margin indicate full marks.

Marks Distribution :

Experiment	:		20
(a) Circuit design / Problem design	:	05	
(b) Implementation	:	10	
(c) Output	:	03	
(d) Discussion	:	02	
Laboratory Notebook	:		04
Viva voce	:		06
Total	:		**30**

Set - I

Answer ***any one*** question.

1. Design a combinational circuit that can add three 1-bit numbers using 2 input NAND gates only.

2. Construct a 1-bit magnitude comparator using 2×4 decoder and other logic gates.

3. Design a full subtractor using 4×1 multiplexer(s) and other logic gates.

4. Implement gated S-R Latch using NAND gates, convert the above into a gated D-Latch.

5. Design a MOD-10 ripple up counter using negative edge triggered JK flip-flop.

6. Design a 4×1 multiplexer using basic gates.

7. Show that a 4×1 multiplexer is a universal building block.

8. Design a 4 input 3 output priority encoder, with one output as valid output indicator.

9. Design a 2 bit comparator using basic Logic gates only.
