2023

COMPUTER SCIENCE — HONOURS — PRACTICAL

Paper : CC-1P

Full Marks : 30

The figures in the margin indicate full marks.

Marks Distribution :

Experiment	:		20
(a) Circuit design / Problem design		: 05	
(b) Implementation		: 10	
(c) Output		: 03	
(d) Discussion		: 02	
Laboratory Notebook	:		04
Viva voce	:		06
Total	:		**30**

Set - II

Answer ***any one*** question.

1. Design a combinational circuit that can add three 1-bit numbers using 2 input NOR gates only.

2. Realize AND, OR, NOT, XOR Logic using NOR gates only.

3. Design a full adder using 4×1 multiplexer(s) and other Logic gates.

4. Convert a D flip-flop into a JK flip-flop.

5. Design a MOD-5 synchronous up counter using JK flip-flops, and other necessary Logic gates.

6. Design a 2×4 active high decoder using basic gates with a provision of an active low type enable input.

7. Design a 4 line to 2 line encoder using basic Logic gates only.

8. Generate Excess – 3 code using a binary parallel adder.

9. Design one 8×1 multiplexer using 4×1 multiplexers only.
