

2025

ELECTRONICS — HONOURS

Paper : DSCC-2

(Operational Amplifiers and Digital Systems)

Full Marks : 75

The figures in the margin indicate full marks.

*Candidates are required to give their answers in their own words
as far as practicable.*

Group - A

1. Answer **any ten** questions : 2×10
- (a) Explain principle of duality in Boolean algebra.
 - (b) What is meant by Common Mode Gain of an OPAMP?
 - (c) Draw and explain the switching equivalent of a NAND gate.
 - (d) State one advantage of the non-inverting mode over the inverting mode of operation of an OPAMP.
 - (e) Add two hexadecimal numbers A3C5 and 7D06.
 - (f) State any two differences between an ideal and a practical OPAMP.
 - (g) Define set-up and hold time of a digital gate.
 - (h) Convert the hexadecimal number 3FE to octal.
 - (i) State two advantages of R-2R converter over binary weighted D-A converter.
 - (j) Design a 2-input EX-OR gate using NAND gates only.
 - (k) Design a 2-input AND gate using 2-input NOR gates only.
 - (l) What is priority encoder?

Group - B

Answer **any three** questions.

2. (a) What is meant by slew rate of an OPAMP? Derive its expression.
- (b) A 741C OPAMP with a slew rate of $0.5V/\mu s$ is used as an inverting amplifier with a gain of 50. If the frequency response is flat up to 20kHz, find the maximum peak to peak input signal that can be applied without distorting the output. (1+2)+2
3. Simplify the following Boolean expression using Karnaugh map : 5
- $F(A, B, C, D) = \Sigma m(0, 1, 3, 5, 6, 7, 8, 9, 10, 12, 14).$

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4. Derive the expression for output voltage and hysteresis voltage of Schmitt trigger using OPAMP. 5
5. Show that a positive logic AND gate is equivalent to a negative logic OR gate and vice versa. $2\frac{1}{2}+2\frac{1}{2}$
6. Write down the truth table of a full adder and design the circuit using NAND gates only. 5

Group - C

Answer *any four* questions.

7. (a) Draw the circuit diagram of an R-2R D/A converter and find expression for its output voltage and resolution.
- (b) A 4 bit R-2R ladder type D/A converter having $R = 10 \text{ k}\Omega$ and $2R = 20 \text{ k}\Omega$ with $V_R = 10\text{V}$. Find its (i) resolution and (ii) I_0 (input current) for a digital input of 1101. $5+(2\frac{1}{2}+2\frac{1}{2})$
8. (a) Derive expression for output voltage of a logarithmic amplifier using OPAMP.
- (b) Derive expression for output voltage of a differential amplifier using OPAMP. 5+5
9. (a) State and prove De Morgan's theorem.
- (b) Write the difference in characteristics of TTL and CMOS logic families.
- (c) What do you mean by Minterms and Maxterms? 4+4+2
10. (a) Realise the POS form of the expression $F = \sum m(1, 2, 5)$.
- (b) Perform the following subtraction using 2's complement method :
 $(10110111)_2 - (10001001)_2$.
- (c) What is meant by 'bouncing' effect in clocked circuits? How can it be avoided? 3+3+(1+3)
11. (a) Design an 8 : 1 multiplexer using 2 : 1 multiplexers only.
- (b) Design (i) a two input OR gate and (ii) a two input NAND gate using 2 : 1 multiplexers only. 4+(3+3)
12. (a) Draw and explain the circuit of a 4-bit shift registers with parallel loading.
- (b) Draw and explain the operation Johnson counter with its timing diagram. 5+5
13. (a) Draw and explain the circuit for a J-K flip-flop.
- (b) Draw and explain the operation of a decade counter.
- (c) What is meant by 'glitch' with respect to a modulo counter? 3+5+2