2025

COMPUTER APPLICATION — VOCATIONAL

Paper : DSCC-1

(Computer Fundamentals and Digital Logic)

Full Marks : 75

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

1. Answer ***any five*** questions : 2×5

(a) Convert decimal $(398)_{10}$ to a 16-bit binary number by first converting to hexadecimal.

(b) Draw the circuit diagram to implement the expression $Y = \left(A\bar{D} + BC\right) \cdot \left(\bar{B} + D\right)$ using two input fundamental gates only.

(c) Draw the Karnaugh map for $Y = \sum m(0, 2, 4, 6, 8) + \sum d(7, 9, 11, 13, 15)$.

(d) Implement an XNOR logic function using just five two-input NAND gates. Illustrate the necessary circuit diagram.

(e) Draw the logical circuit diagram of 1 to 2 decoder designed using fundamental logic gates only.

(f) What is the highest clock frequency that a 4-bit asynchronous up counter can support, given that each flip-flop in it has a propagation delay of 50 nanoseconds?

(g) What does the term 'race-around condition' refer to in-relation to flip-flops?

(h) Highlight four main differences between Assembly Language and Machine-level Language programming.

Answer ***any three*** questions. 5×3

2. Simplify the Boolean expression $Y = \bar{A} \cdot \bar{B} \cdot C + \bar{A} \cdot B \cdot \bar{C} \cdot D + A \cdot \bar{B} \cdot C \cdot D + A \cdot B \cdot C \cdot D + A \cdot B \cdot C \cdot \bar{D}$ using Karnaugh map and realise the simplified expression using fundamental logic gates. Draw the appropriate circuit diagram.

3. Cascade two 2 to 4 decoders with active low enable input to form a 3 to 8 decoder. Include the truth table and briefly describe its operation. Use fundamental logic gates if required to realize the circuit.

4. Illustrate the circuit diagram for a clocked D flip-flop, provide a concise explanation of its operation and include its truth table.

5. Draw the logical circuit diagram of 4 bit Serial-In-Serial-Out (SISO) shift register using D flip-flop and explain its function in brief.

6. What is Read-Only Memory (ROM)? What limitations of ROM led to the development of Programmable Read-Only Memory (PROM)? Also, explain the applications of both ROM and PROM.

Answer ***any five*** questions.

7. Design a 3-bit asynchronous up counter using negative edge-triggered JK flip-flops. Draw the state transition diagram and explain the design steps, including the suitable logic circuit diagram. 6+2+2

8. How can a Master-Slave flip-flop be built using JK flip-flops? Write its truth table, explain how it works, and draw the logic circuit diagram. 4+3+3

9. Realize $Y = A + BC\bar{D}$ using two input NAND logic gates and $Y = (A+C)(A+\bar{D})(A+B+\bar{C})$. 5+5

10. (a) Realize a 4-bit controlled inverter using XOR logic gates. Explain its operation.

    (b) Design a 4-bit 2's complement subtractor using 4-bit parallel adder and other necessary logic gates and explain its operation with the help of an example. 3+7

11. What is a full adder? Illustrate its truth table, derive simplified expressions for the Sum and Carry out, and depict the logical circuit diagram. 3+3+2+2

12. Design a 4 to 1 multiplexer using fundamental logic gates. Draw the functional table and the characteristic equation. 5+3+2

13. Convert a D flip-flop into a JK flip-flop. Illustrate the excitation table, elucidate the conversion process and provide the logical circuit diagram. 3+4+3

14. Implement the function $F(A, B, C, D) = \Sigma m(3, 4, 5, 6, 7, 9, 10, 12, 14, 15)$ using a 4 to 1 multiplexer along with other required logic gates. Explain the design process, create the truth table, derive the simplified expression and provide the logical circuit diagram. 3+2+3+2