2025

COMPUTER SCIENCE — MDC

Paper : CC-1

(Computer Fundamentals and Digital Logic)

Full Marks : 75

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

Answer ***question nos.*** **1 & 2** and ***any five*** questions from the rest.

1. Answer ***any five*** questions of the following : 2×5

(a) Highlight the main differences between Combinational and Sequential Circuits.

(b) What is Race-around Condition?

(c) What is Decoder?

(d) Find the Hexadecimal representation of $(723)_8$.

(e) What is De Morgan's theorem, and how can the first theorem be proved using a truth table.

(f) Why the NAND gate is a Universal Gate?

(g) Simplify the following Expression : $X = (\overline{A} + B)\cdot(A+B+D).\overline{D}$.

(h) What is K-map (Karnaugh)?

2. Answer ***any three*** from following :

(a) What is Full Adder? Design a Full Adder using basic logic gates and draw the appropriate logic circuit diagram. 2+3

(b) Draw the logical circuit diagram of clocked T flip-flop using NAND logic gates only. 5

(c) Convert S-R Flip-Flop into D Flip-Flop. 5

(d) Mention the differences between Multiplexer and Demultiplexer. 5

(e) Implement the Boolean function using 8×1 multiplexer and if required use basic logic gates only.

$F(A, B, C, D) = \sum m(0, 1, 3, 4, 5, 8, 9, 15)$ 5

3. Cascade 8 to 1 multiplexers to realize a 16 to 1 multiplexer along with other mecessary logic gates. Draw the logic circuit diagram. 5+5

Please Turn Over

4. (a) Write short note on Supercomputers.

   (b) What is System Software? What are the differences between system and application software?

   (c) What is Virus? What are the steps that can be taken to detect and prevent it from affecting Computer Systems? 3+3+(1+3)

5. (a) Draw the state diagram of JK flip-flop.

   (b) Compare Synchronous Sequential Circuit with Asynchronous Sequential Circuit. 6+4

6. Design a MOD-7 asynchronous down counter using T flip-flop and other necessary logic gates. Draw the logical circuit diagram. Explain the design procedure and draw the truth table. 3+4+3

7. (a) Design a half adder with truth table.

   (b) Design a three-bit full adder using NAND gates only. Draw the truth table. 4+6

8. Simplify the logical expression using Karnaugh Map in SOP and POS form :

   $F(A, B, C, D) = \sum m(0, 2, 3, 6, 7) + \sum d (2, 5, 6, 11)$. 5+5

9. Design a BCD to EXCESS-3 code converter using basic logic gates only. 10

10. Design a full subtractor circuit using a 3-to-8 decoder, with additional basic logic gates only if necessary. Draw the truth table. 5+5