2025

COMPUTER SCIENCE — MINOR

Paper : MN-1

(Computer Fundamentals and Digital Logic)

Full Marks : 75

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

Answer ***question no.* 1, 2** and ***five*** questions from the rest.

1. Answer ***any five*** questions : 2×5

(a) (i) Convert $(1100)_2 \rightarrow (?)_{10}$

(ii) Convert $(210B)_{16} = (?)_{10}$

(b) Define Modulo Counter.

(c) How can a decoder be used as a demultiplexer?

(d) Realize Ex-NOR using NOR logic gates.

(e) What is meant by Clock Pulse?

(f) Realize $F = \Sigma_m(1, 2, 5, 6)$ using multiplexers.

(g) What is De-bouncer?

(h) What are the differences between combinational and sequential circuits?

Section – A

2. Answer ***any three*** questions :

(a) Implement a 1-bit comparator circuit using NAND gates. Draw the necessary logical circuit diagram. 3+2

(b) $Y = \Sigma_m(0, 1, 9, 10, 13, 14) + \Sigma_d(2, 3)$, Minimize this logic expression by K-map and implement using logic gates. Draw the truth table. 2+2+1

(c) Design a D flip-flop using logic gates. Explain the circuit using relevant illustrations. 3+2

(d) Implement $F = \Sigma_m(1, 2, 5, 6, 8, 9, 11)$ using 8×1 multiplexer with proper illustrations. 5

(e) Realize Ex-OR function using NAND logic gates only. 5

Section – B

3. (a) How can an SR flip-flop be converted into a JK flip-flop? Illustrate the conversion with appropriate logic diagram.

   (b) Convert JK flip-flop to T flip-flop. Explain with proper illustrations. 5+5

4. Design a 4-bit code converter that transforms a binary code into its corresponding Excess-3 code, and illustrate the implementation with a suitable logic circuit diagram using basic gates. Draw the necessary truth table. 6+4

5. (a) How can a full adder be realized using 4 to 1 multiplexer along with the necessary logic gates? Illustrate the design with a suitable logic diagram.

   (b) Realize a half subtractor using 4 to 1 multiplexers only. Illustrate the design with a suitable logic diagram. (3+4)+(1+2)

6. (a) Design a 8×1 multiplexer using 4×1 multiplexer only.

   (b) Design a 8×1 multiplexer using 2×1 multiplexer only. Explain the circuit in each case. 5+5

7. (a) Design an asynchronous MOD-10 counter with proper illustrations.

   (b) Draw timing diagram. 8+2

8. Design a synchronous counter capable of counting the states →

   $0 \rightarrow 1 \rightarrow 2 \rightarrow 3 \rightarrow 4 \rightarrow 0$

   Explain with proper illustrations. 8+2

9. Implement 3×8 decoder using 2×4 decoders with suitable diagram. 8+2

10. (a) Design a Master-Slave J-K flip-flop. Draw the corresponding truth table.

    (b) What is race-around condition? 8+2
