2026

PHYSICS — HONOURS

Paper : DSCC-13

(Electronics - II)

Full Marks : 75

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

1. Answer ***any five*** questions : 3×5

(a) Subtract $(1011)_2$ from $(11100)_2$ using 2's complement method of subtraction.

(b) Draw circuit diagram of OR gate using n-p-n transistors and resistances.

(c) Implement the boolean expression $X = AB + \bar{A}C$ using NAND gates only.

(d) Cascade two half adders to construct a full adder.

(e) Design a 8:1 multiplexer using two 4:1 multiplexers.

(f) Draw the circuit diagram of a clocked SR-Flip-Flop.

(g) What is the output after two clock pulses for a bit sequence 1101 serially entered into a 4-bit parallel-out shift register which is initially clear?

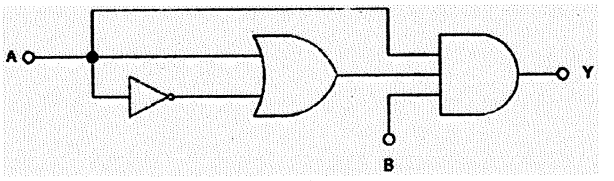
(h) Design a twisted ring counter (4-bit).

Answer ***any five*** questions.

2. (a) Evaluate the sum of $(8)_{16} + (F)_{16} = (?)_{16}$.

(b) Design a NOT-gate using a transistor ($\beta_{sat} = 50$) considering $V_{CE\ sat} = 0.2V$, $I_C = 5$ mA and source voltage = 5 volt., V_{BE} (ON) = 0.8 V.

(c) Obtain the Boolean expression for the output Y in the following logic circuit :



Simplify the expression and show that the circuit is equivalent to an AND gate with inputs A and B. Construct it using NAND gates only. 2+4+(3+2+1)

Please Turn Over

3. (a) Simplify the following Boolean expression in SOP form using Karnaugh Map :

$$F(A,B,C,D) = \sum m(0,1,3,5,7,8,9,11,13,15).$$

(b) Implement the above simplified expression using basic gates.

(c) Implement XOR gate using NOR gates only and give its truth table.

(d) Prove the Boolean expression : $\bar{A}B\bar{C} + \bar{A}BC + AB\bar{C} + ABC = B$. 3+2+(3+2)+2

4. (a) Draw the full substractor circuit using basic gate only. Also, write its truth table.

(b) Draw the block diagram of a 4-bit binary adder subtractor and explain its operation.

(c) Differentiate between combinational and sequential circuits with two examples each. (2+2)+4+(2+2)

5. (a) Implement the following Boolean expression using 8:1 multiplexer :

$$F(A,B,C) = \sum m(2,4,6,7)$$

How can you use a 8:1 multiplexer to implement a logical expression with four inputs?

(b) What is a demultiplexer? Draw the block diagram of a 4 to 16 line demultiplexer.

(c) For a design of (16:1) multiplexer, how many select lines will be required? (3+2)+(3+2)+2

6. (a) What is the basic difference between SR Flip-Flop and JK Flip-Flop?

(b) Draw the circuit diagram of JK Flip-Flop and explain its operation using sequence table.

(c) Implement a D-Flip-Flop using JK Flip-Flop.

(d) Convert an SR Flip-Flop into a JK Flip-Flop. [circuit diagram only] 2+(2+3)+3+2

7. (a) What is the basic difference in operation between MS-JK and JK Flip-Flop? Explain with block diagram.

(b) Why is JK Flip-Flop called an one-bit register? Explain the utility of PRESET and CLEAR operation in Flip-Flop in this regard.

(c) What is the difference between positive and negative edge triggering? Which type of triggering can be implemented using these triggering? (2+2)+(2+2)+(2+2)

8. (a) What do you mean by a counter?

(b) Design a 4-bit ripple counter using JK Flip-Flop. Convert it into MOD-10 counter.

(c) Draw the block diagram of a 4-bit SISO type shift register and explain its operation using sequence table. 2+(3+2)+(2+3)

9. (a) Draw the block diagram of D/A conversion circuit.

(b) A 5-bit D/A converter produces $V_{out} = 0.2V$ for a digital input of 00001. Find the value of V_{out} for an input 1111.

(c) "A synchronous counter is faster than an asynchronous counter" — Justify the statement.

(d) Design a 3-bit synchronous counter and explain its operation. 3+3+2+(2+2)
