

2026

COMPUTER SCIENCE — HONOURS

Paper : DSCC-6

(Microprocessor and Its Applications)

Full Marks : 75

The figures in the margin indicate full marks.

*Candidates are required to give their answers in their own words
as far as practicable.*

1. Answer **any five** questions : 2×5
- (a) What is the function of carry flag in 8085?
 - (b) Name the non-maskable hardware interrupt in 8085 and state its function.
 - (c) Briefly explain the conceptual difference between a Machine Cycle and an instruction T-state.
 - (d) How many bits are there in address bus and data bus of 8085 microprocessor?
 - (e) State the status of $\overline{IO/\overline{M}}$, S1 and S0 during memory read machine cycle.
 - (f) How many T-states are required to execute the following 8085 instructions : MVI B, 05 H & INX H?
 - (g) How does the 8085 processor use the RESET IN signal to re-initialize its internal states and registers?
 - (h) Under what scenario or condition is the Auxiliary Carry (AC) flag bit set to 1 during arithmetic processing?

Answer **any three** questions.

- 2. Explain different addressing modes of 8085 with suitable examples. 5
- 3. Discuss how the state of the status flags influences conditional branching and contrast this with unconditional branching using relevant instruction mnemonics. 5
- 4. Explain the address-data bus de-multiplexing with suitable illustrations. 5
- 5. (a) Differentiate between CALL and JMP instructions in 8085. Explain the execution of CALL instruction with example. 3
(b) What are the specific functions of the CLK (OUT) and X1, X2 pins connected to the timing and control unit block? 2
- 6. Explain the generation of Control Signals with suitable illustrations. 5

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Answer *any five* questions.

7. (a) Draw the timing diagram of LDA 8000H assuming that the instructions are written across the memory locations 9000H, 9001H and 9002H.
(b) Explain the following instructions with examples :
(i) LXI H, (data)₁₆
(ii) STAX, B. 6+4
8. (a) What is memory mapped I/O scheme?
(b) Interface a 4 kbyte EPROM with microprocessor 8085 in the memory range F000H and FFFFH. Provide a suitable circuit diagram to illustrate this interfacing. 2+8
9. (a) Explain the operations of PUSH and POP instructions with proper illustrations.
(b) What is the significance of RST 5.5, RST 6.5 and RST 7.5 interrupts? 5+5
10. Draw the internal architecture of 8085 microprocessor and explain each section in brief. 5+5
11. (a) Trace the register and flag transformations for the following code. Determine the final value in registers and the state of the Zero (Z) flag upon reaching the halt phase :
MVI A, 08H
MVI C, 00H
Loop: RRC
JNC Skip
INR C
Skip: DCR A
JNZ Loop
HLT
(b) Explain the precise functionality and internal byte configurations of the SIM (Set Interrupt Mask) and RIM (Read Interrupt Mask) instructions. 5+5
12. (a) What are the differences between 'Burst mode' and 'Cycle stealing' techniques of DMA data transfer scheme?
(b) Explain why a DMA controller (8257/8237) is necessary for high speed data transfer, detailing the cycle-stealing data transfer mode. 5+5
13. (a) Detail the functional differences between the RESET IN and RESET OUT pins of the microprocessor 8085.
(b) What specific category of information is stored inside the stack pointer register?

(3)

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- (c) Suppose the Accumulator contains the byte value 5AH. Show the step-by-step binary contents of the Accumulator and the state of the Carry flag (CY) after executing the following instructions sequentially :

1. RLC
2. RAL
3. STC

2+2+6

14. Write short notes on the following (*any two*) :

5+5

- (a) BSR mode of 8255(PPL)
 - (b) I/O mapped I/O
 - (c) Foldback memory
 - (d) Flag register of 8086.
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